LISTING OF CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently amended) A process ~~Process~~ for forming a housing for electronic modules, ~~in particular sensors, integrated circuits and optoelectronic components;~~ comprising the steps of:

providing a substrate ~~(1) which has~~ having one or more regions, the one or more regions ~~comprising~~ having a structure selected from the group consisting of semiconductor structures, ~~(2) and comprising~~ connection structures, structures ~~or~~ for forming semiconductor structures, ~~(2)~~ and structures for forming connection structures, ~~(3) and of which~~ the substrate having at least a first substrate side ~~(1a) is~~ to be encapsulated and an underside~~,~~;

providing a vapor-deposition glass source ~~(20),~~;

arranging the first substrate side ~~(1a)~~ in such a manner with respect to the vapor-deposition glass source that the first substrate side ~~(1a)~~ can be vapor-coated;

vapor-coating the first substrate side with a glass layer (4);

thinning the substrate ~~(1)~~ on the underside ~~(1b) ,~~;

producing etching pits on the underside ~~(6),~~; and

producing line contacts ~~(7)~~ on the underside ~~(1b)~~.

2. (Currently amended) The process as claimed in claim 1, wherein the one or more regions ~~having semiconductor structures (2)~~ are arranged on the first substrate side ~~(1a) of the substrate~~.

3. (Currently amended) The process as claimed in claim 2, further comprising providing ~~wherein~~ the substrate ~~is provided~~ with a passivation layer ~~(10, 11)~~ on a second side ~~(1b), which~~ that is on the opposite side from the first substrate side ~~(1a)~~.

4. (Currently amended) The process as claimed in ~~one of the preceding claims~~ claim 1, wherein the substrate ~~comprising~~ comprises a wafer, ~~wherein~~ the process ~~comprises the~~ further comprising packaging of components which still form part of ~~a~~ the wafer.

5. (Currently amended) The process as claimed in ~~one of the preceding claims, wherein the substrate (1) is vapor-coated with a~~ claim 1, further comprising vapor-coating a second substrate side with the glass layer ~~(4, 10, 11) on two sides (1a, 1b)~~.

6. (Currently amended) The process as claimed in ~~one of the preceding claims~~ claim 1, wherein ~~a~~ the vapor-deposition glass source ~~(20) which~~ generates at least a binary glass system ~~is provided~~.

7. (Currently amended) The process as claimed ~~in one of the preceding claims~~ claim 1, wherein the ~~vapor-deposition glass source (20) is operated until~~ first substrate side is vapor-coated until the glass layer ~~(4)~~ has a thickness in the range from 0.01 to 1000 µm~~, in particular~~ on the first substrate side.

8. (Currently amended) The process as claimed in ~~one of the preceding claims~~ claim 1, wherein ~~as part of~~ the step of providing ~~a~~ the vapor-deposition glass source ~~(20),~~ comprises providing a reservoir ~~comprising~~ having organic constituents ~~is provided~~, and ~~these~~ converting the organic constituents ~~are converted~~ into the vapor state through application of a vacuum or through heating~~,~~ so that during the vapor-coating mixed layers comprising inorganic and organic constituents can be formed on the first substrate side.

9. (Currently amended) The process as claimed in ~~one of the preceding claims~~ claim 1, wherein the glass layer has a thickness ~~is~~ in the range between 0.1 and 50 µm.

10. (Currently amended) The process as claimed ~~in one of the preceding claims~~ claim 1, wherein the glass layer has a thickness ~~is~~ in the range between 50 and 200 µm.

11. (Currently amended) The process as claimed in ~~one of the preceding claims~~ claim 1, wherein ~~the vapor-deposition glass of the source (20) is generated~~ vapor-coating the first substrate side with the glass layer comprises generating a vapor from a glass target ~~(23)~~ by means of an electron beam ~~(24)~~.

12. (Currently amended) The process as claimed in ~~one of the preceding claims~~ claim 11, wherein the ~~vapor-deposition glass used~~ glass target is a borosilicate glass ~~containing~~ comprising aluminum oxide and alkali metal oxide fractions.

13. (Currently amended) The process as claimed in ~~one of the preceding claims~~ claim 1, wherein the ~~vapor-deposition~~ glass layer has a coefficient of thermal expansion ~~which~~ that is virtually equal to that of the substrate.

14. (Currently amended) The process as claimed in ~~one of the preceding claims~~ claim 1, wherein the glass layer ~~(4) is produced with~~ has a thickness ~~which is required for~~ sufficient to provide a hermetic seal~~, and wherein a layer of plastic (5) is applied above the glass layer (4) in order to facilitate further processing of the substrate (1)~~.

15. (Currently amended) The process as claimed in ~~one of the preceding claims, wherein~~ claim 1, further comprising vapor deposting a plurality of glass layers ~~are vapor-deposited~~ onto the substrate ~~(1), it being possible for the glass layers to consist of various glass compositions~~.

16. (Currently amended) The process as claimed in ~~one of the preceding claims, wherein the further processing of the substrate (1) involves the removal of~~ claim 1, further comprising removing material from a second substrate side ~~(1b)~~, the second substrate side being ~~which is~~ on the opposite side from the first substrate side ~~(1a)~~.

17. (Currently amended) The process as claimed in ~~one of the preceding claims~~ claim 1, wherein the substrate ~~(1)~~ includes a wafer having a plurality of ~~semiconductor~~ the structures ~~(2) and connection structures (3), with the second substrate side (1b), which is on the opposite side from the first substrate side (1a), being thinned, the pits (6) being etched on the second substrate side (1b) in the region of the connection structures to be produced, the regions for forming the semiconductor structures (2) being lithographed using plastic layers, line contacts (7) being produced on the second substrate side (1b) in the regions having connection structures (3), the plastic being removed from the second substrate side (1b), a ball grid array (8) being applied at the line contacts (7), and~~ wherein the process further comprises dividing the wafer ~~being divided up so as~~ to form a plurality of electronic modules which each have first[[,]] encapsulated sides ~~(1a)~~.

18. (Currently amended) The process as claimed in claim 38 ~~17~~, further comprising providing the underside ~~wherein the second substrate side (1b) is provided~~ with a plastic covering ~~(10)~~ while leaving clear the ball grid ~~regions (8)~~ array.

19. (Currently amended) The process as claimed in claim ~~17 or 18~~ 39, ~~wherein~~ further comprising vapor coating the underside with the glass layer after the plastic layers ~~has~~ have been removed from the ~~second substrate side (1b)~~ underside ~~the whole of the second substrate side is vapor-coated with a glass layer (11), and wherein the line contacts (7) are uncovered by local elimination of the glass layer (11), after which the steps of applying the ball grid array (8)~~ and ~~of~~ dividing up the wafer ~~are carried out in order to obtain~~ so that the plurality of electronic modules ~~which~~ are encapsulated on both sides.

20. (Currently amended) The process as claimed in claim 19, wherein the ~~entire second substrate side is vapor-coated with a~~ glass layer ~~(11) with~~ on the underside has a thickness in the range from 1 to 50 µm~~, and~~.

21. (Currently amended) The process as claimed in ~~one of claims 17 to 20, wherein~~ claim 36, further comprising filling in the etching pits ~~(6) which lead to the connection structures (3) are filled~~ with conductive material ~~(12), after which, with or without removal of the plastic (10) from the second substrate side (1b) and with or without a glass layer (11) on the second substrate side (1b), and leaving clear the line contacts (7), the ball grid array (8) is applied at the line contacts (7) and/or at the filling material~~.

22. (Currently amended) The process as claimed in ~~one of the preceding claims~~ claim 1, wherein ~~the~~ vapor-coating ~~of~~ the first substrate side ~~(1a)~~ with ~~a~~ the glass layer ~~(4)~~ comprises plasma ion assisted deposition ~~(PIAD)~~.

23. (Currently amended) An electronic module, ~~in particular as a sensor or as an integrated circuit or as an optoelectronic component, producible by the process as claimed in one of the preceding claims~~ comprising:

a substrate having a first substrate side and a second substrate side opposite the first substrate side;

one or more semiconductor structures and/or connection structures being disposed on the first substrate side;

a glass layer being deposited on the first substrate side; and

a plurality of etched pits and line contacts being defined in the second substrate side.

24. (Currently amended) The electronic module as claimed in claim 23, further comprising ~~which on a first side (1a) has one or more regions with semiconductor structures (2), and connection structures (3), wherein the substrate is coated with a vapor-deposited~~ the glass layer ~~(4) on at least one side~~ being deposited on the second substrate side.

25. (Currently amended) The electronic module as claimed in claim 24, ~~wherein~~ further comprising a plastic layer ~~(5) which~~ that reinforces the module ~~is applied to~~ on the glass layer ~~(4)~~.

26. (Currently amended) The electronic module as claimed in ~~one of claims 24 or 25~~ claim 23, wherein the ~~substrate~~ second substrate side is thinned after the glass layer is deposited on the first substrate side.

27. (Currently amended) The electronic module as claimed in ~~one of claims 24 to 26, wherein the substrate is provided with~~ claim 23, further comprising a passivation layer ~~(10, 11)~~ on ~~a~~ the second substrate side ~~(1b), which is on the opposite side from a first side (1a) having semiconductor structures and connection structures~~.

28. (Currently amended) The electronic module as claimed in ~~one of claims 24 to 27~~ claim 23, wherein the glass layer ~~(4)~~ comprises a mixed layer of inorganic and organic constituents.

29. (Currently amended) The electronic module as claimed in ~~one of claims 24 to 28, which includes~~ claim 23, wherein the glass layer comprises a ~~multilayer~~ plurality of glass layers ~~(4)~~.

30. (Currently amended) The electronic module as claimed in claim 29, wherein the individual layers of the plurality of glass layers have different compositions.

31. (Currently amended) The electronic module as claimed in ~~one of claims 24 to 30~~ claim 23, ~~wherein the substrate (1), on a second side (1b), has~~ further comprising line contacts that are connected to the one or more semiconductor structures and/or connection structures on the first substrate side ~~(1a)~~.

32. (Currently amended) The electronic module as claimed in claim 31, ~~which includes~~ further comprising a ball grid array ~~(8)~~ at the line contacts.

33. (Cancelled)

34. (New) The process as claimed in claim 1, further comprising applying a layer of plastic above the glass layer.

35. (New) The process as claimed in claim 15, wherein the plurality of glass layers have the same or various glass compositions.

36. (New) The process as claimed in claim 17, wherein the etching pits are produced on the underside opposite the structure.

37. (New) The process as claimed in claim 17, wherein the line contacts are produced on the underside opposite the structure.

38. (New) The process as claimed in claim 17, further comprising applying a ball grid array at the line contacts.

39. (New) The process as claimed in claim 17, further comprising lithographing plastic layers on the substrate to define the structure and removing the plastic layers from the underside.

40. (New) The process as claimed in claim 39, wherein removing the plastic layers from the underside comprises uncovering the line contacts by local elimination of the glass layer.